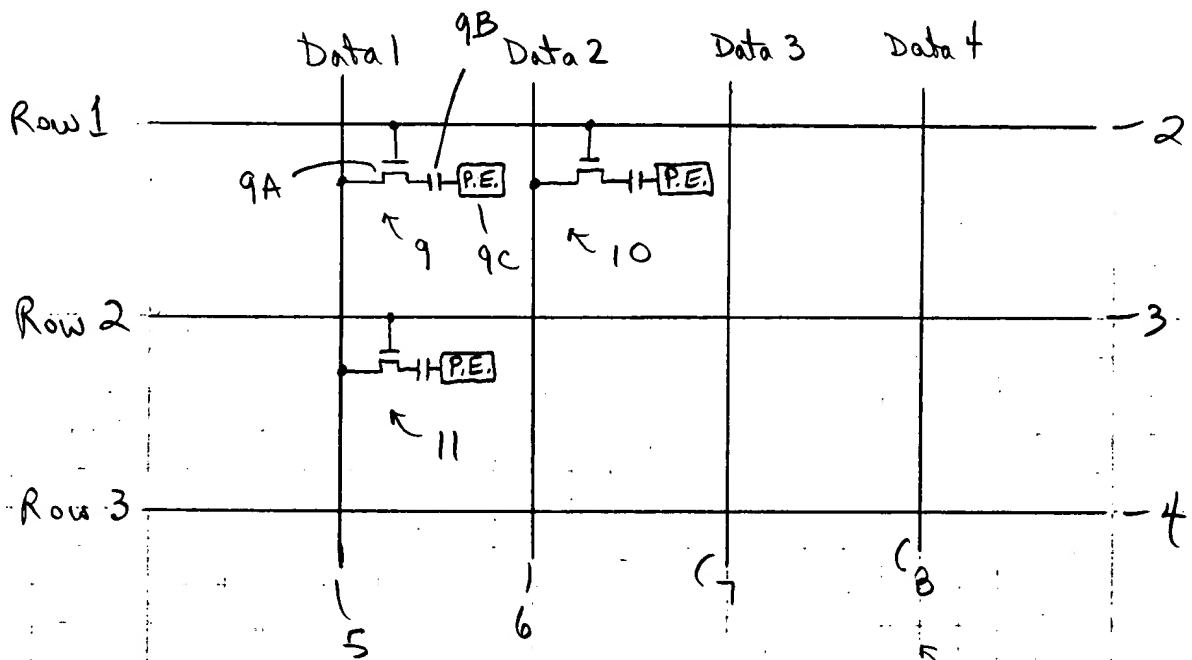


FIG. 1 (Prior Art)



500 SHEETS, FILLER 5 SQUARE  
 400 SHEETS, FILLER 5 SQUARE  
 300 SHEETS, FILLER 5 SQUARE  
 200 SHEETS, FILLER 5 SQUARE  
 100 SHEETS, FILLER 5 SQUARE  
 50 SHEETS, FILLER 5 SQUARE  
 25 SHEETS, FILLER 5 SQUARE  
 10 SHEETS, FILLER 5 SQUARE  
 5 SHEETS, FILLER 5 SQUARE  
 2 SHEETS, FILLER 5 SQUARE  
 1 SHEET, FILLER 5 SQUARE  
 100 RECYCLED WHITE 5 SQUARE  
 42-392 100 RECYCLED WHITE 5 SQUARE  
 42-399 200 RECYCLED WHITE 5 SQUARE  
 Made in U.S.A.



00260-05372900

FIG. 2A

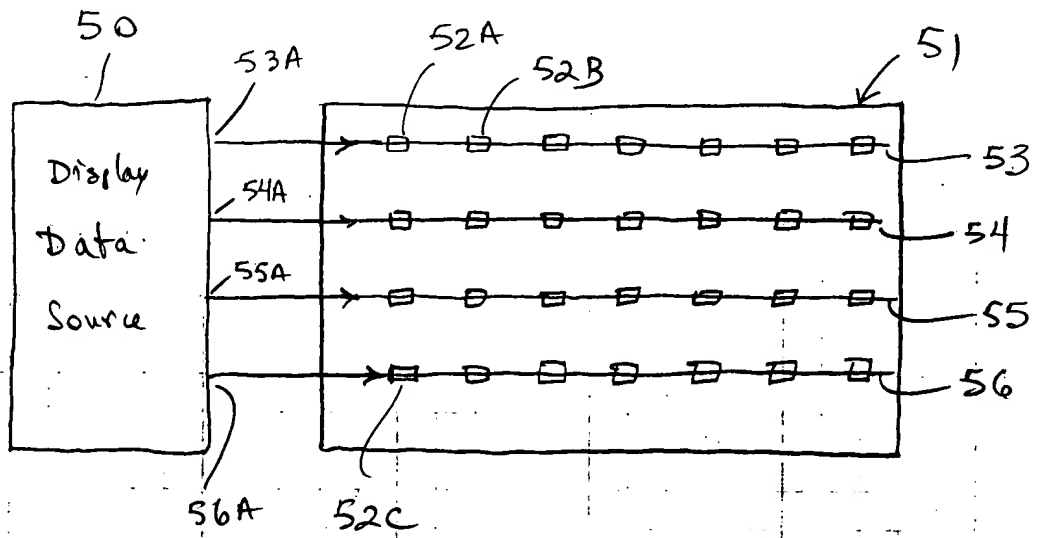
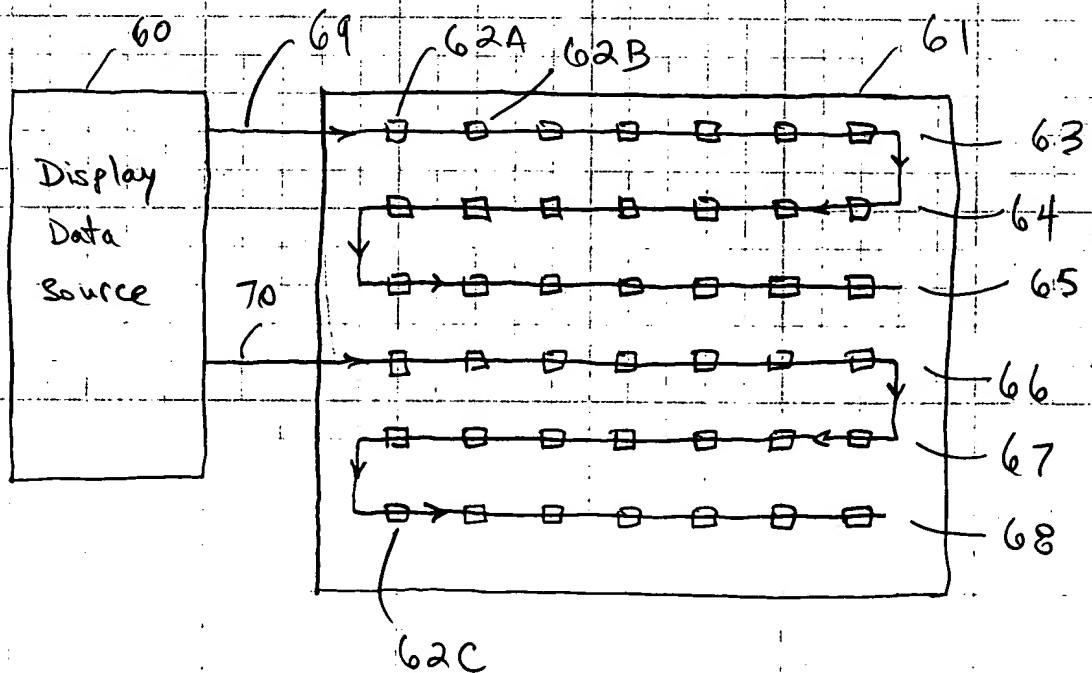


FIG. 2B












FIG. 3A

Pixel Data (101) → Display Driver 102

Display Driver 102 → Display Driver 103

Display Driver 103 → 100

The diagram shows a 4x4 grid of P.E. blocks connected to the Display Driver 102. The Display Driver 103 is connected to another 4x4 grid of P.E. blocks. The output of the Display Driver 103 is labeled 100.

Fig. 3B

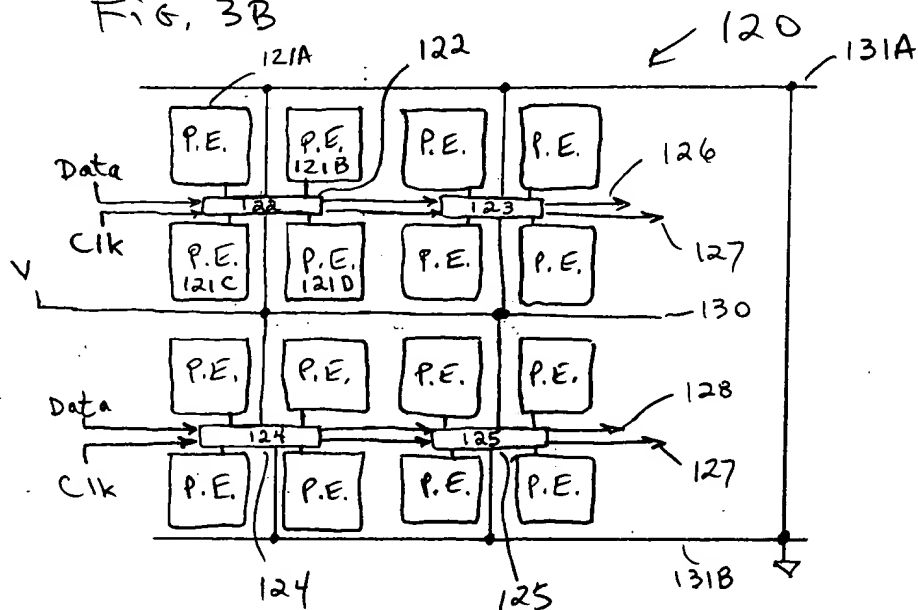


FIG. 3C

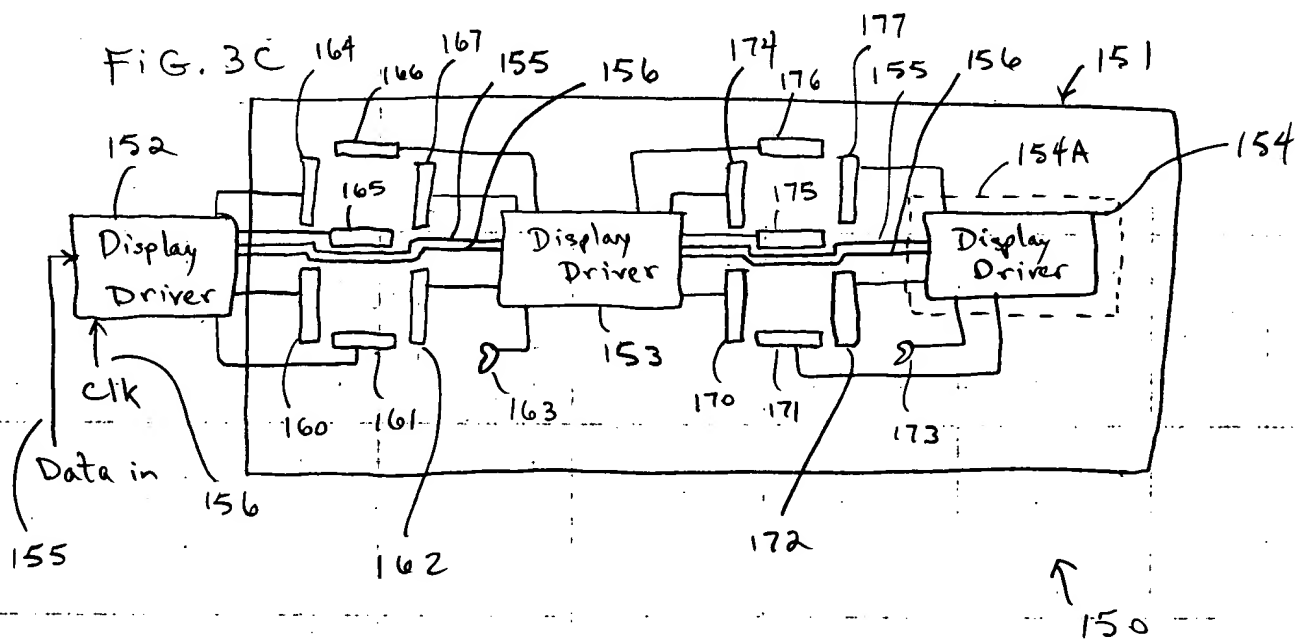
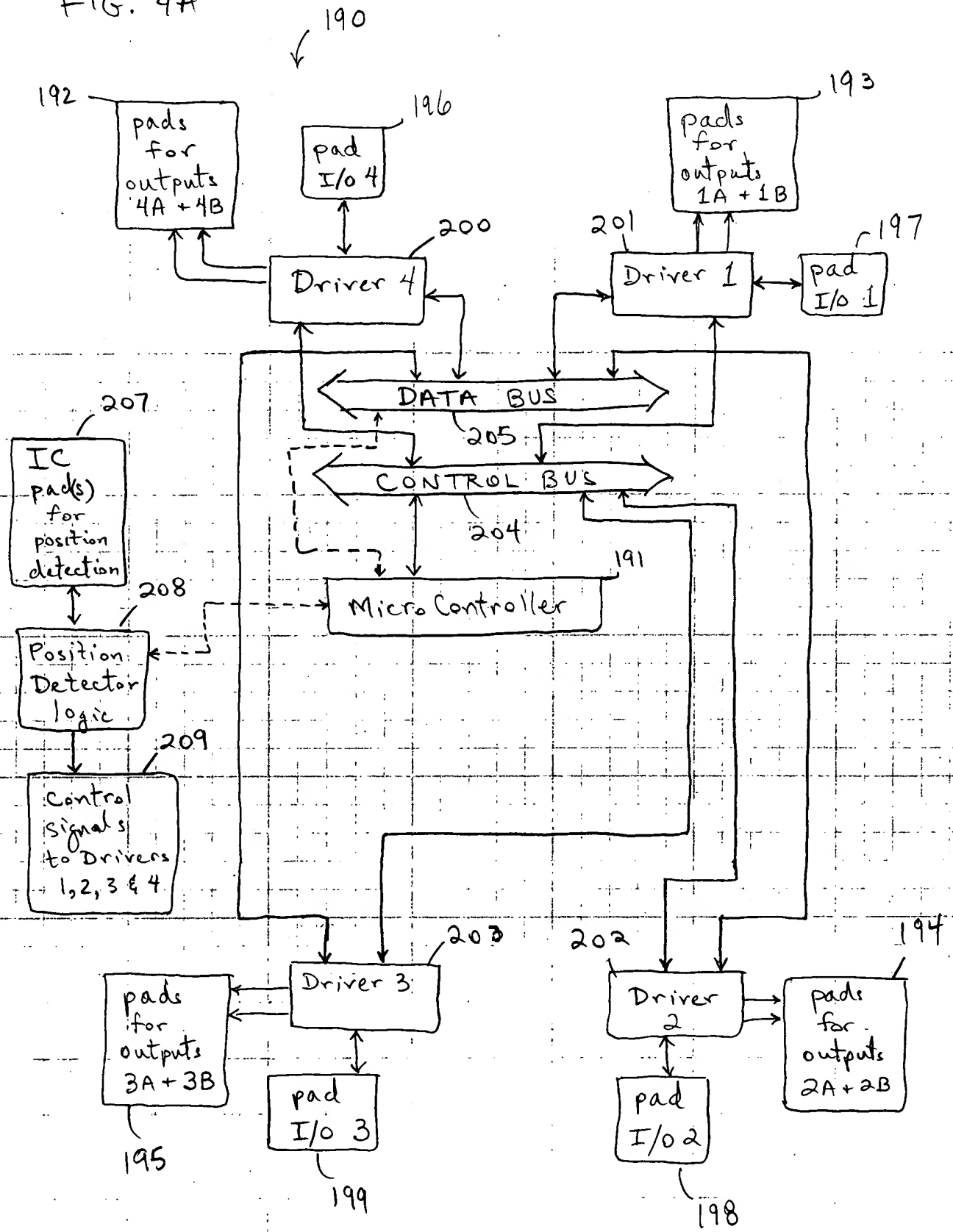




FIG. 4A



230

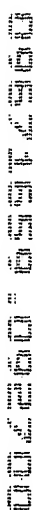


FIG. 4C

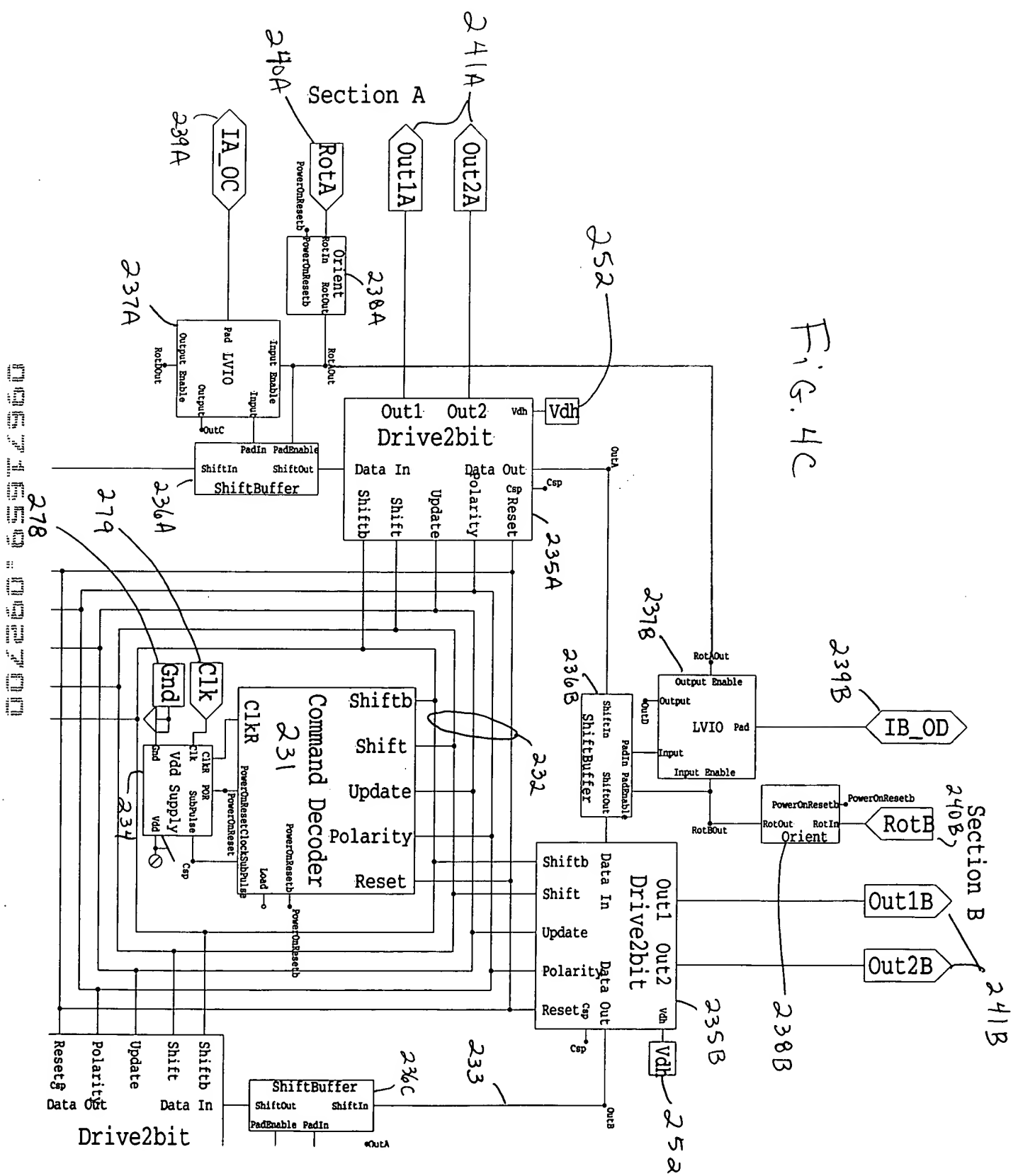




FIG. 5A

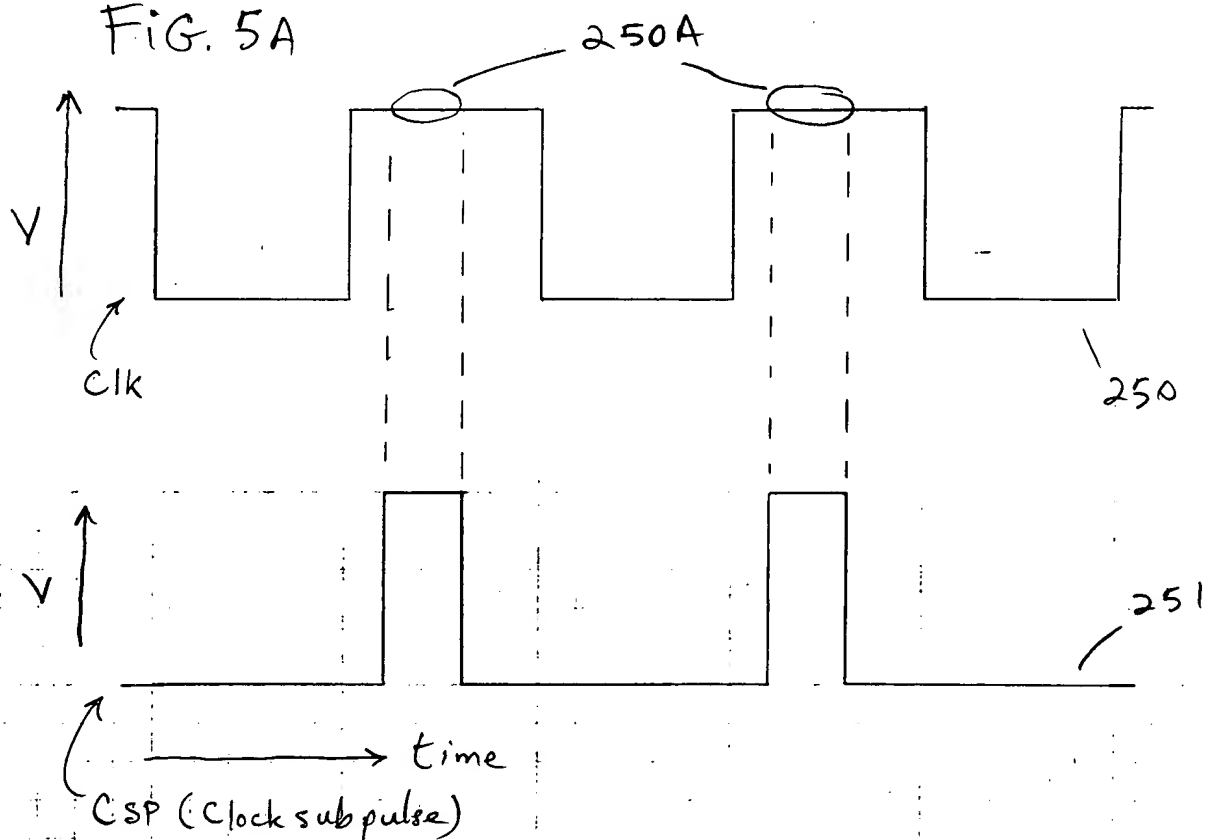


FIG. 5B

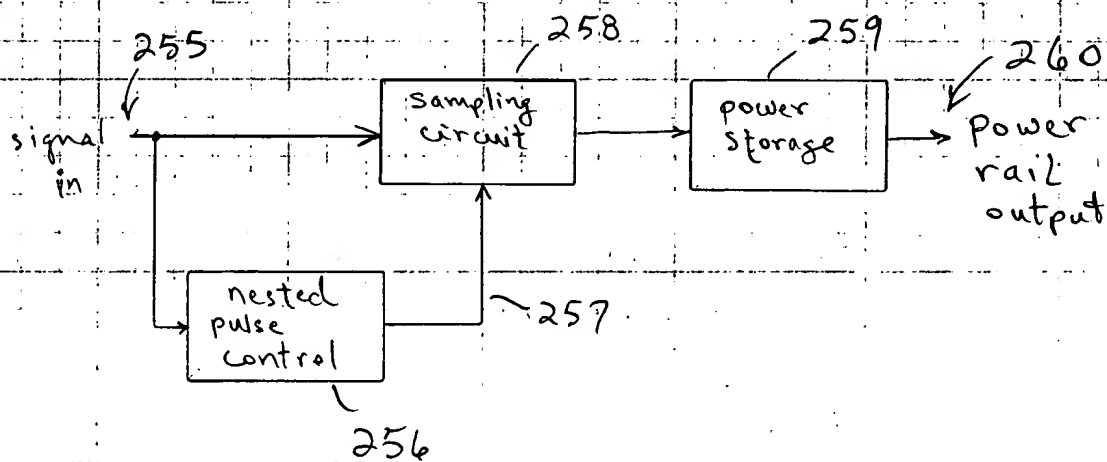
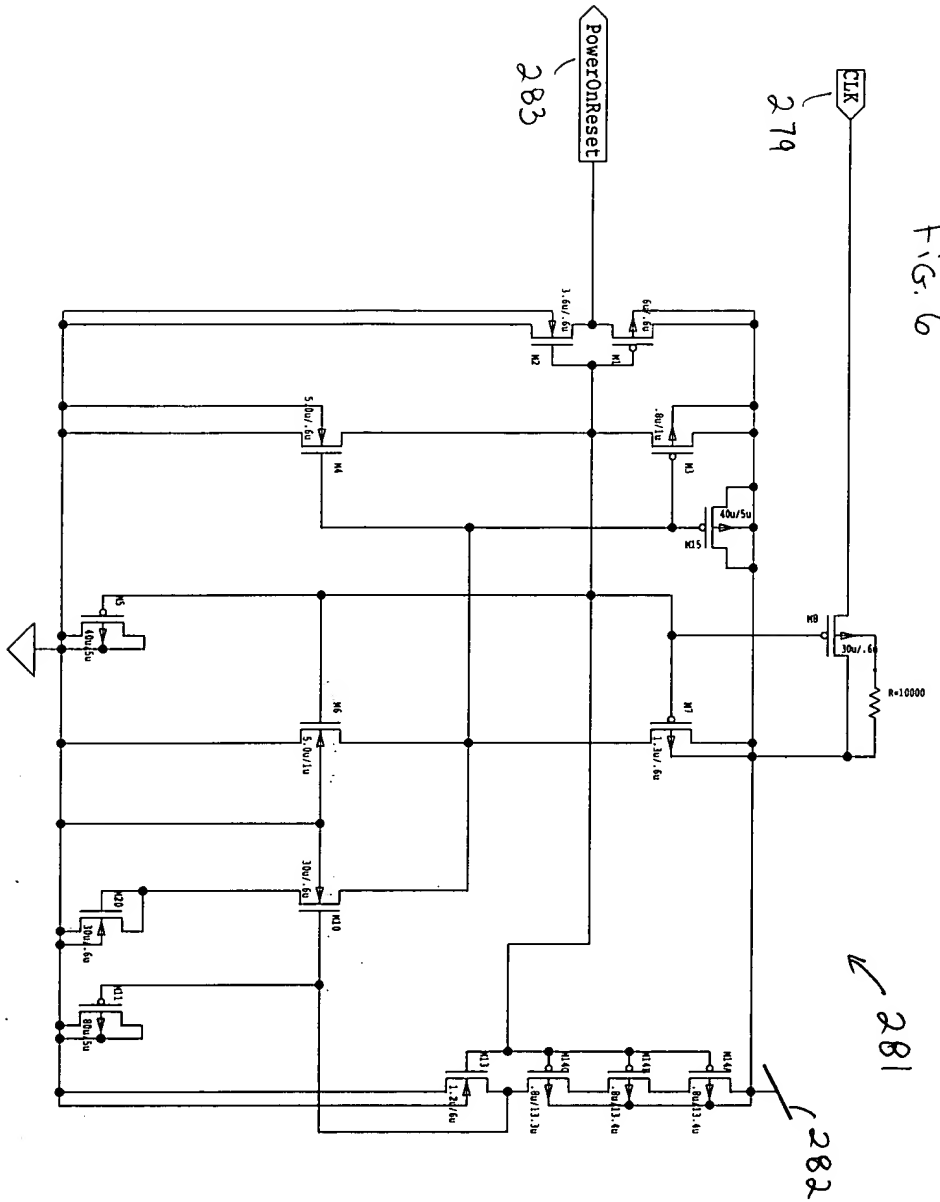


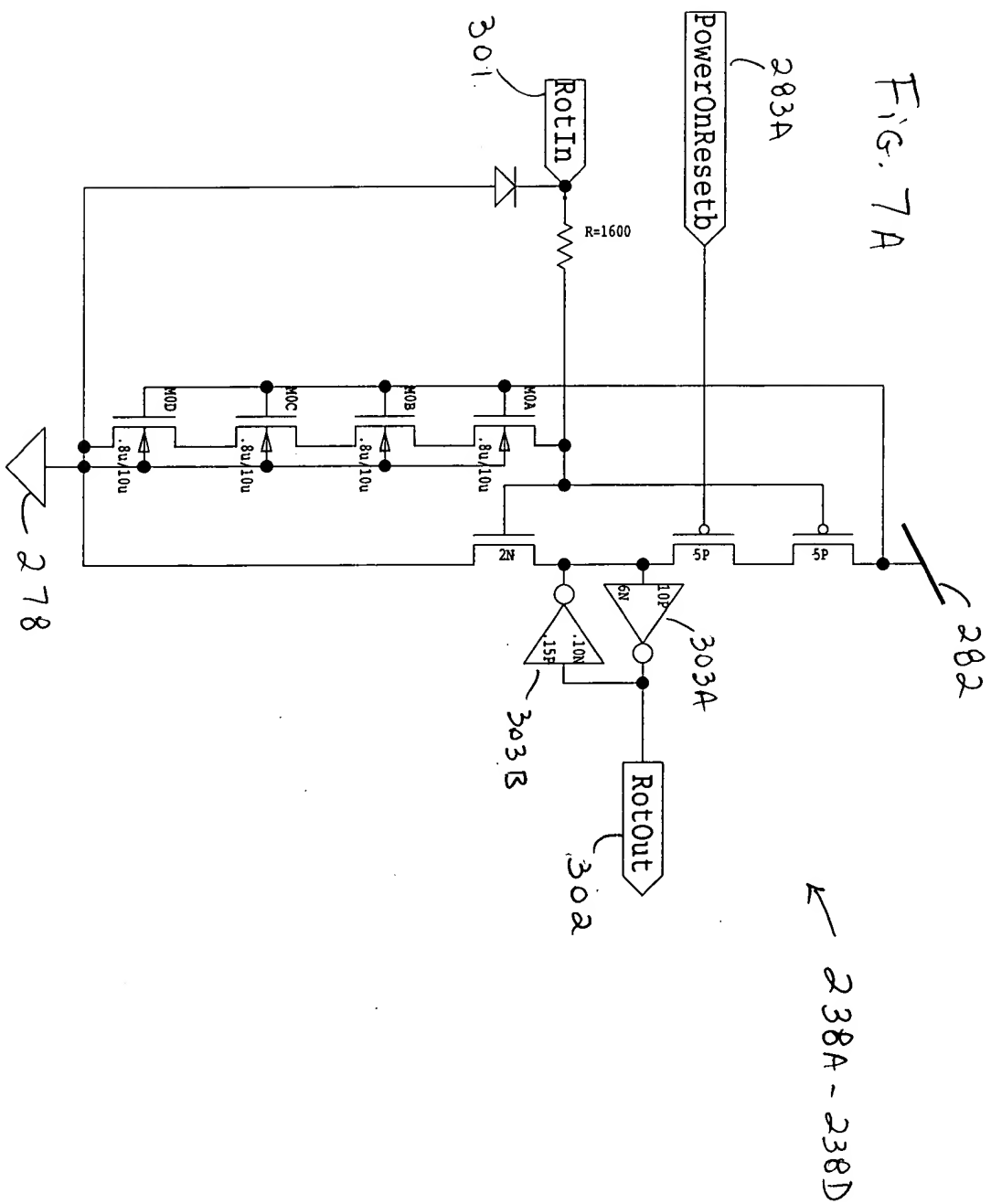


FIG. 6



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Fig. 7A



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FIG. 7B

308 311 312 306 311 312 307 309 305 311 312

A cross-sectional view of a semiconductor device. A substrate 305 is shown with a trench 306. Inside the trench is an integrated circuit (IC) 311. A layer 308 is formed on the top surface of the substrate 305, extending over the trench 306.

237A-237D

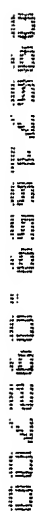


FIG. 9A

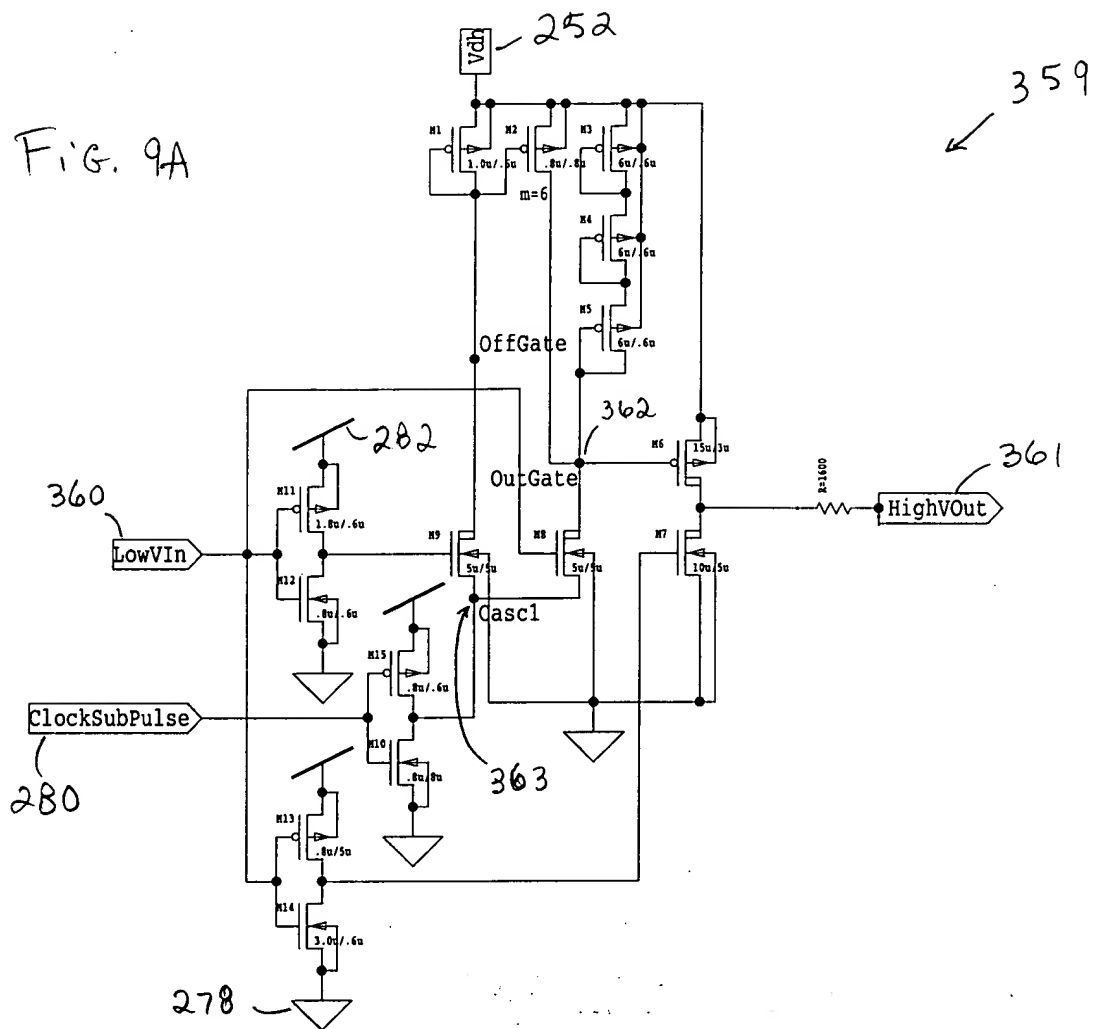
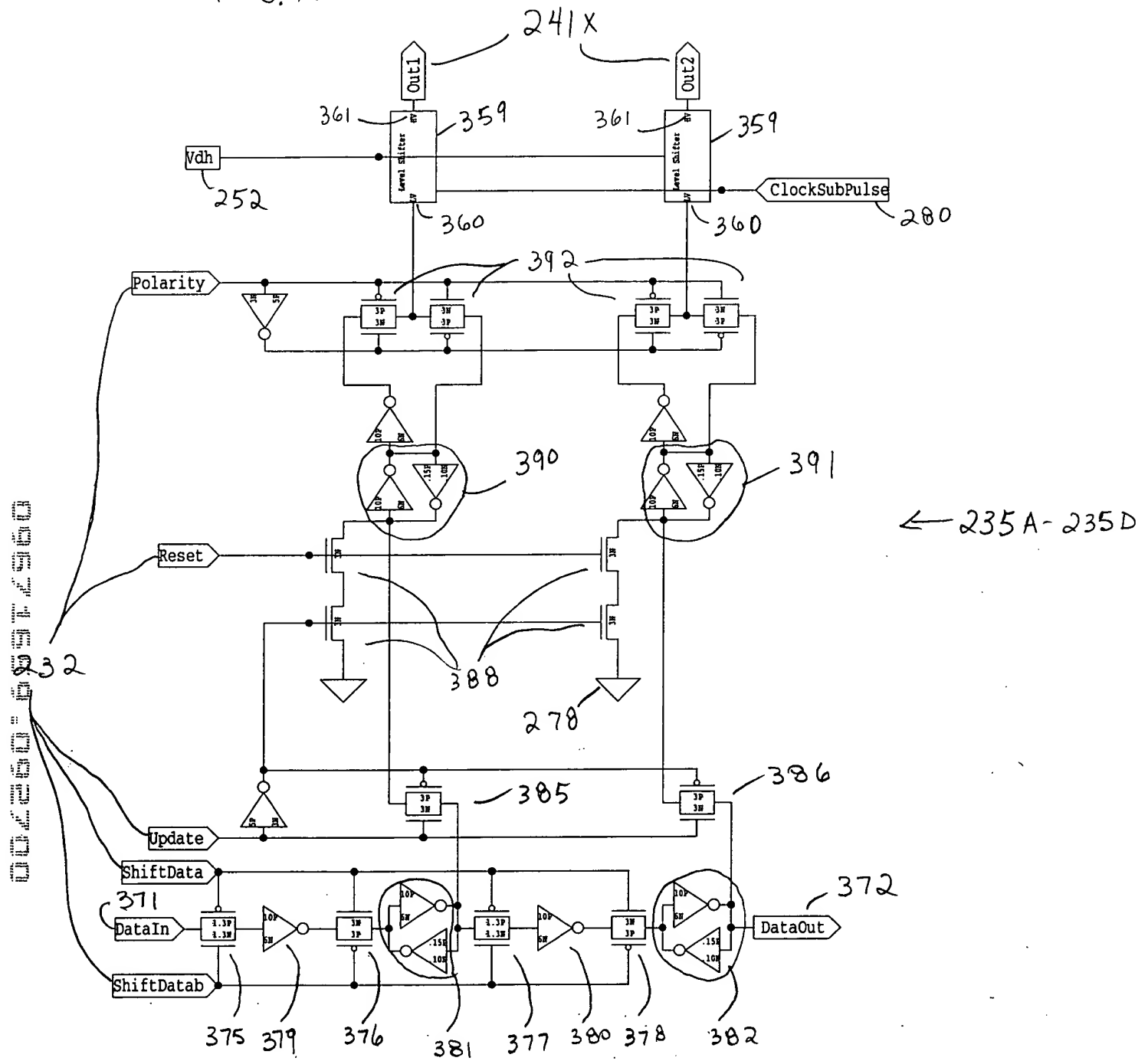


FIG. 10





231

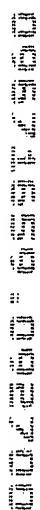


FIG. 11B

Command Decoder Timing

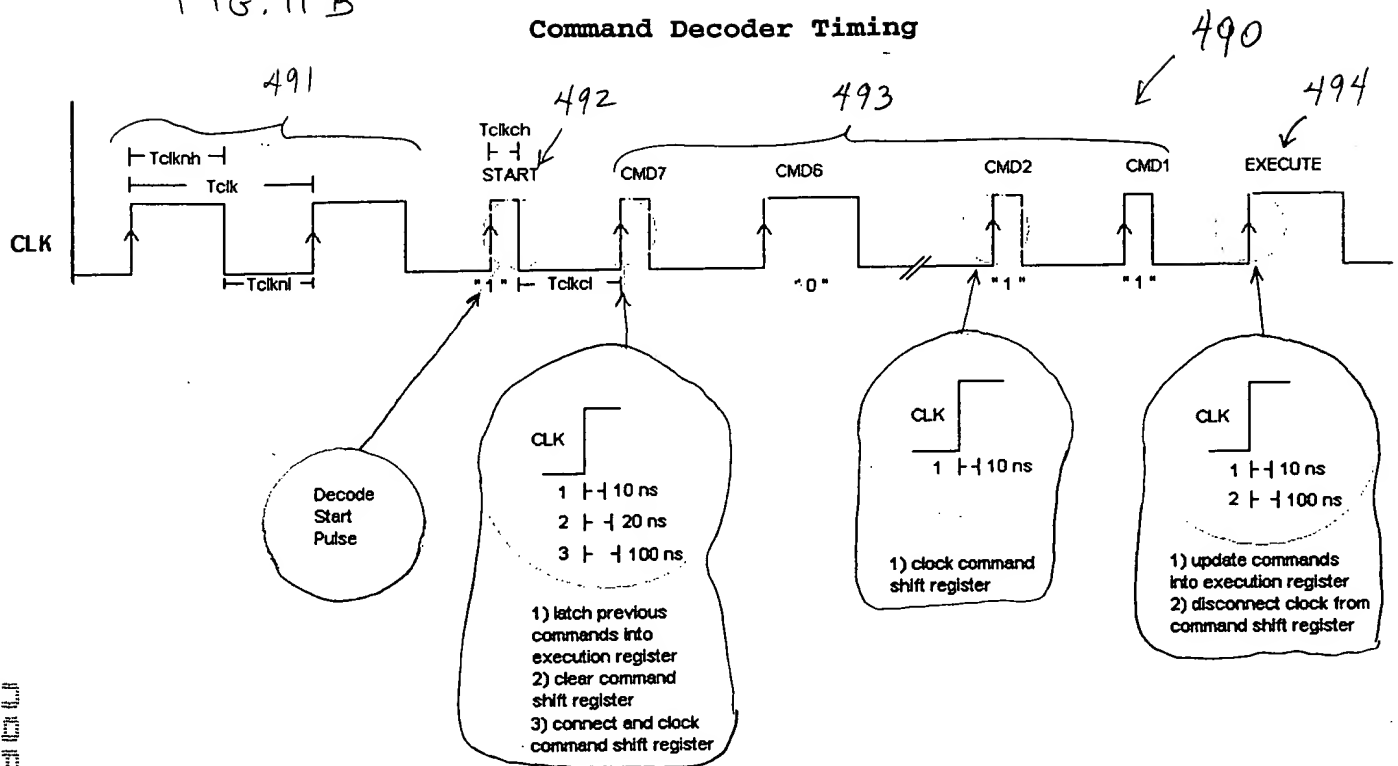
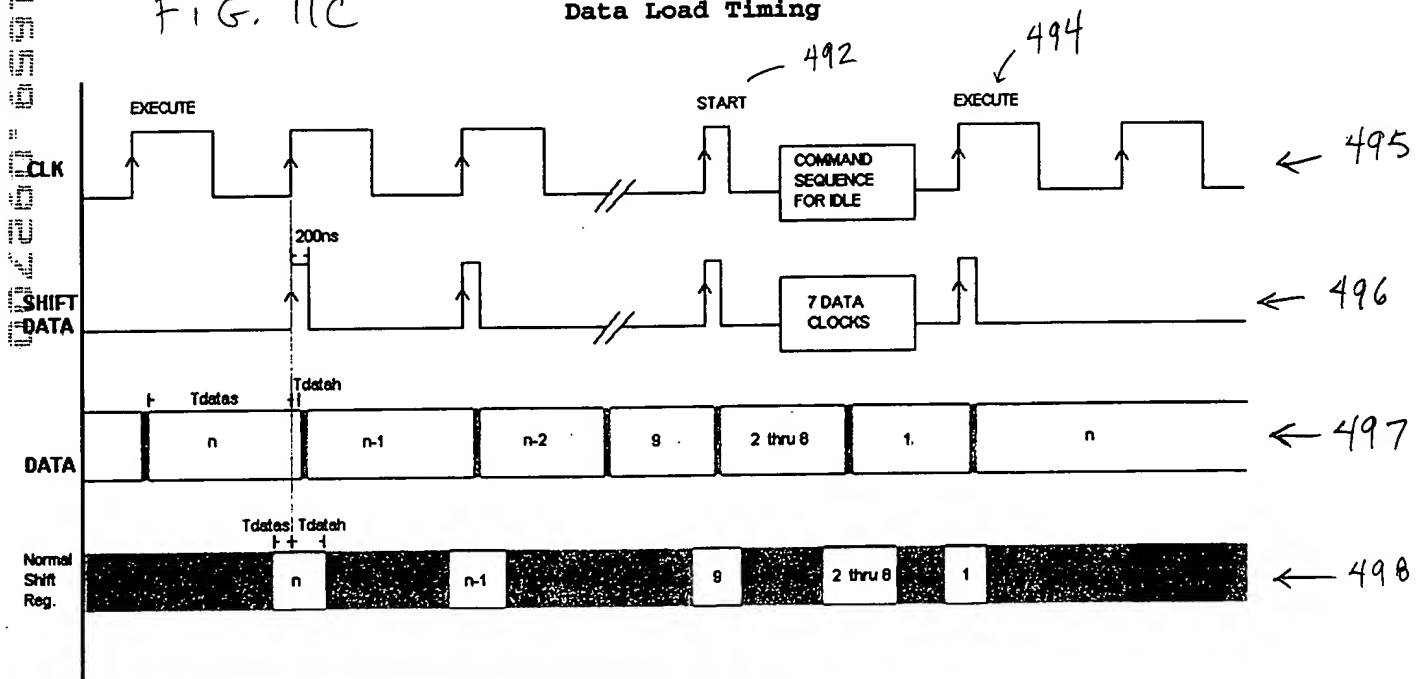


FIG. 11C

Data Load Timing



- n is the total number of data values for all daisy-chained device blocks. (example:  $n = 32$  for 4 device blocks).
- data must be low upon start-up and through the first command sequence.

500 SHEETS, FILLER 5 SQUARE  
50 SHEETS EYE-EASE® 5 SQUARE  
100 SHEETS EYE-EASE® 5 SQUARE  
200 SHEETS EYE-EASE® 5 SQUARE  
100 RECYCLED WHITE 5 SQUARE  
200 RECYCLED WHITE 5 SQUARE

501

502

503

50.4

505

[illegible]

FIG 11 E

520

521

522

[illegible]

The diagram illustrates two identical integrated circuit (IC) blocks, each containing a complex internal logic structure. Key components within each block include buffers (e.g., Buff1, Buff2), multiplexers (e.g., Mux1, Mux2), registers (e.g., Reg1, Reg2), and various control logic elements (e.g., And, Or, Not). The blocks are interconnected via a shared Data In bus at the top and a shared Data Out bus at the bottom. A common clock signal (CLK) is provided to both blocks. Specific pins or internal nodes are labeled with reference numerals: 239A, 240A, 239B, 252, 241A, 278, and 279. The entire assembly is identified by the label "To additional Display IC circuits".

Display IC circuits  
To additional Driver

Year	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

५७०

[illegible]

FIG. 14B

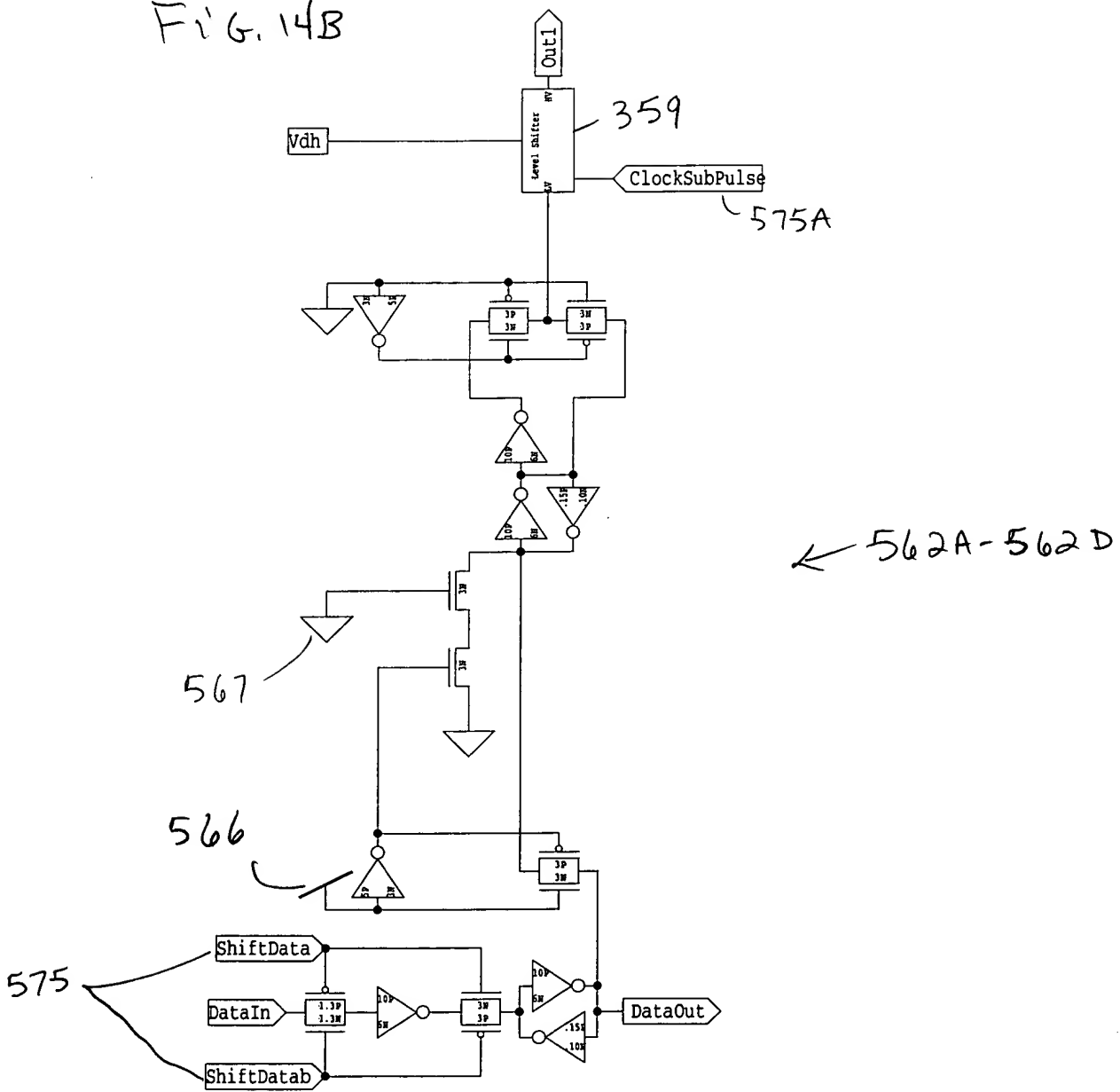
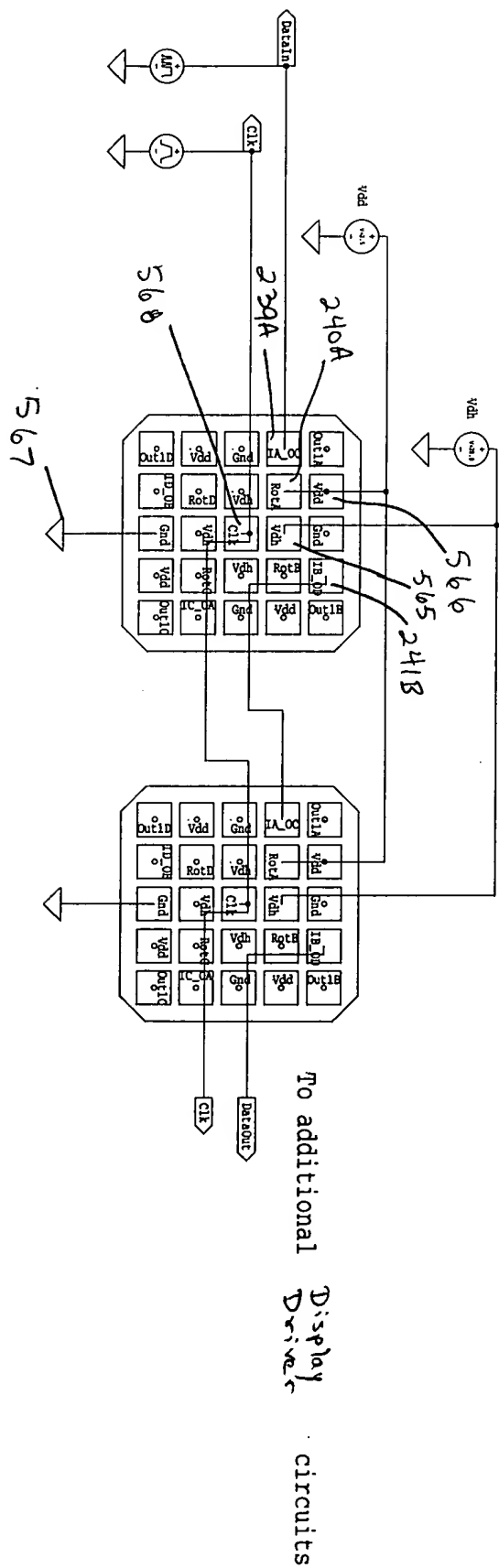






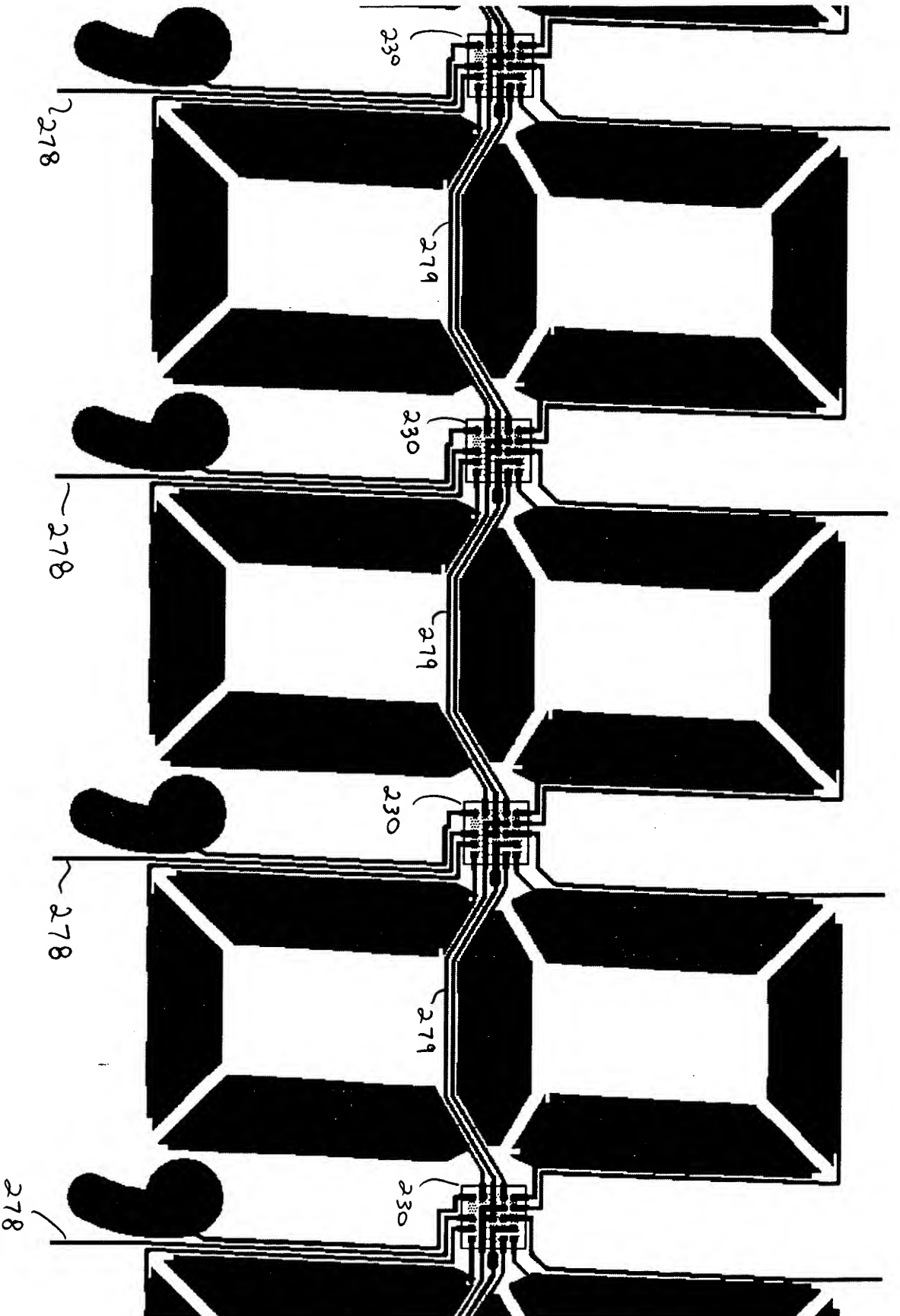
FIG. 14D



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FIG. 15B



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